

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
13 January 2005 (13.01.2005)

PCT

(10) International Publication Number
WO 2005/003880 A3

(51) International Patent Classification⁷: **H04J 3/06**

(21) International Application Number:
PCT/IL2004/000575

(22) International Filing Date: 29 June 2004 (29.06.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/484,294 3 July 2003 (03.07.2003) US

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(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,

AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,
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KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD,
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TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM,
ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI,
SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, ML, MR, NE, SN, TD, TG).

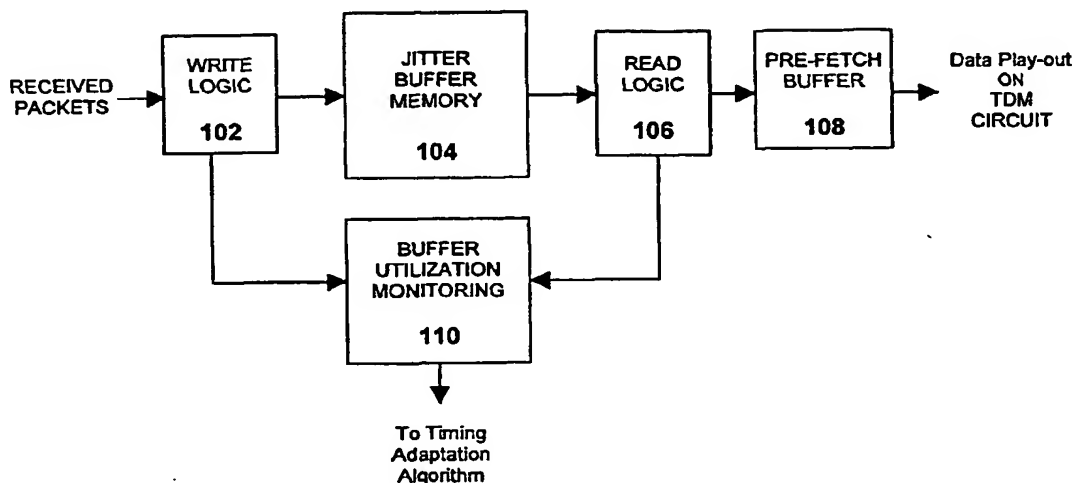
Published:

- with international search report
- before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR PARTITIONING ALLOCATION AND MANAGEMENT OF JITTER BUFFER
MEMORY FOR TDM CIRCUIT EMULATION APPLICATIONS

100



(57) Abstract: A method for partitioning allocation and management of a jitter buffer memory for TDM circuit emulation applications comprises the steps of obtaining a channel hierarchy for a plurality of packet carrying channels having different channel rates, obtaining a packet sequential number, and using the channel hierarchy and the packet sequential number, generating a base-address in the jitter buffer memory. Each channel is allocated a space in the buffer memory that is proportional to its rate, and out-of-order packets are automatically reordered by the jitter buffer.

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(88) Date of publication of the international search report:
14 April 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IL04/00575

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H04J 3/06

US CL : 370/516

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/516,517,907;375/371,372

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 2003/0227943 A1 (HALLMAN ET AL) 11 December 2003 (11.12.2003), page 1, paragraph 0006-0007; page 4, paragraph 0054-0055; Figure 20.	1-19
A,P	US 6,665,317 B1 (SCOTT) 16 December 2003 (16.12.2003), column 2, lines 1-20.	1-19
A, P	US 2003/0219012 A1 (WISLER et al) 27 November 2003 (27.11.2003), page 1, paragraph 0008.	1-19

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☐ See patent family annex.

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Date of the actual completion of the international search

19 January 2005 (19.01.2005)

Date of mailing of the international search report

01 MAR 2005

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Alexandria, Virginia 22313-1450

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